Notice of References Cited	Application/Control No. 10/007,498	Applicant(s)/Patent Under Reexamination NGUYEN ET AL.	
	Examiner Latha Ravindran	Art Unit 2183	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-5,826,055	10-1998	Wang et al.	712/218
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Motorola, MPC7410 RISC Microprocessor Technical Summary, 2000, Pages 2 - 11, 20 - 21, 31 - 33, 36
	V	Morris, John, Computer Architecture The Anatomy of Modern Processors, 1998, http://ciips.ee.uwa.edu.au/~morris/CA406/pipelines.html
	W	LSI Logic Corporation, An Overview of the ZSP Architecture White Paper, 2000
	X	Ruetz, Peter and Wen-Wi Ti, Interleaved Multiplier Accumulator, September 12, 1992, European Patent Application

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.